ICS ADVENT

ISA/PCI BACKPLANES
Product Manual

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Errata Sheet

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- **Page 2-1, 2-3:** The model number 15005-02 listed for the five-slot backplane is incorrect. The model number should be 15002-02.

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FOREWORD

This product manual provides information to install, operate and or program the referenced product(s) manufactured or distributed by ICS Advent. The following pages contain information regarding the warranty and repair policies.

Check our Web site (***http://www.icsadvent.com/techsupport***) for technical information, manual, andBIOS updates. Technical assistance is also available at: **800-480-0044** (U.S. and Canada) or **858-677-0877** (international).

Manual errors, omissions, bugs, and/or comments: A Customer Comments section is included at the end of this manual. If you experience any problems with the manual or just want to give us some feedback, please review the information in this section. It will tell you how to easily access our web site and provide immediate feedback online.

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Guarantee

A thirty day money-back guarantee is provided on all **standard** products sold. **Special order products** are covered by our Limited Warranty, *however they may not be returned for refund or credit. EPROMs, RAM, Flash EPROMs or other forms of solid electronic media are not returnable for credit - but for replacement only. Extended Warranty available. Consult factory.*

Refunds

In order to receive refund on a product purchase price, the product must not have been damaged by the customer or by the common carrier chosen by the customer to return the goods, and the product must be returned complete (meaning all manuals, software, cables, etc.) within 30 days of receipt and in as-new and resalable condition. The **Return Procedure** must be followed to assure prompt refund.

Restocking Charges

Product returned *after* 30 days, and *before* 90 days, of the purchase will be subject to a **minimum** 20% restocking charge and any charges for damaged or missing parts.

Products not returned within 90 days of purchase, or products which are not in as-new and re-saleable condition, are not eligible for credit return and will be returned to the customer.

Limited Warranty

Effective April 1, 1998, all products carry a two-year limited warranty with the exception of the "Performance Series" I/O products, which are warranted to the original purchaser for as long as they own the product, subject to all other conditions below, including those regarding neglect, misuse and acts of God. Within one year of purchase, ICS Advent will repair or replace, at our option, any defective product. At any time after one year, we will repair or replace, at our option, any defective "Performance Series" I/O product sold. This does not include products damaged in shipment, or damaged through customer neglect or misuse. ICS Advent will service the warranty for all standard catalog products for the first year from the date of shipment. After the second year, for products not manufactured by ICS Advent, the remainder of the manufacturer's warranty, if any, will be serviced by the manufacturer directly.

The **Return Procedure** must be followed to assure repair or replacement. ICS Advent will normally return your replacement or repaired item via Second Day Air. *Overnight delivery or delivery via other carriers is available at additional charge.*

The limited warranty is void if the product has been subjected to alteration, neglect, misuse, or abuse; if any repairs have been attempted by anyone other than ICS Advent or its authorized agent; or if the failure is caused by accident, acts of God, or other causes beyond the control of ICS Advent or the manufacturer. Neglect, misuse, and abuse shall include any installation, operation, or maintenance of the product other than in accordance with the owners' manual.

No agent, dealer, distributor, service company, or other party is authorized to change, modify, or extend the terms of this Limited Warranty in any manner whatsoever. ICS Advent reserves the right to make changes or improvements in any product without incurring any obligation to similarly alter products previously purchased.

Shipments not in compliance with this Guarantee and Limited Warranty Return Policy will not be accepted by ICS Advent.

Return Procedure

For any Limited Warranty or Guarantee return, please contact ICS Advent's Customer Service at **1-800-480-0044** and obtain an Return Material Authorization (RMA) Number. All product(s) returned to ICS Advent for service or credit **must** be accompanied by a Return Material Authorization (RMA) Number. Freight on all returned items **must** be prepaid by the customer who is responsible for any loss or damage caused by common carrier in transit. Returns for Warranty **must** include a Failure Report for each unit, by serial number(s), as well as a copy of the original invoice showing date of purchase.

To reduce risk of damage, returns of product must be in an ICS Advent shipping container. If the original container has been lost or damaged, new shipping containers may be obtained from ICS Advent Customer Service at a nominal cost.

Limitation of Liability

In no event shall ICS Advent be liable for any defect in hardware or software or loss or inadequacy of data of any kind, or for any direct, indirect, incidental, or consequential damages in connection with or arising out of the performance or use of any product furnished hereunder. ICS Advent liability shall in no event exceed the purchase price of the product purchased hereunder. The foregoing limitation of liability shall be equally applicable to any service provided by ICS Advent or its authorized agent.

Some *Sales Items* and *Customized Systems* are **not** subject to the guarantee and limited warranty. However, in these instances any deviations will be disclosed prior to sales and noted in the original invoice. ***ICS Advent reserves the right to refuse returns or credits on software or special order items.***

Advisories

Three types of advisories are used throughout the manual to stress important points or warn of potential hazards to the user or the system. They are the Note, the Caution, and the Warning. Following is an example of each type of advisory:

Note: The note is used to present special instruction, or to provide extra information which may help to simplify the use of the product.

CAUTION!

A Caution is used to alert you to a situation which if ignored may cause injury or damage equipment.

WARNING!

A Warning is used to alert you of a situation which if ignored will cause serious injury.

Cautions and Warnings are accented with triangular symbols. The exclamation symbol is used in all cautions and warnings to help alert you to the important instructions. The lightning flash symbol is used on the left hand side of a caution or a warning if the advisory relates to the presence of voltage which may be of sufficient magnitude to cause electrical shock.

Use caution when servicing any electrical component. We have tried to identify the areas which may pose a Caution or Warning condition in this manual; however, ICS Advent does not claim to have covered all situations which might require the use of a Caution or Warning.

You must refer to the documentation for any component you install into a computer system to insure proper precautions and procedures are followed.

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Chapter 1: Description

ICS Advent ISA/PCI passive backplanes include several models that suit a variety of applications. This chapter describes the backplanes' features, configurations, construction, and connectors.

Features

- Four- or six-layer printed circuit board, depending on model
- Extremely high EMI and RFI noise immunity
- Accepts power connectors from standard PC bus power supplies
- Accepts CPUs with PCI local bus extensions and standard ISA bus CPUs
- Bus Power Check™ LED indicators for +3.3, +5, -5, +12, -12 VDC supplies
- Allows use of standard ISA bus and PCI local bus option cards
- Bus mastering supported on all PCI slots
- Bus-terminating resistor sockets included

Each model has one to four CPU slots, one to 15 ISA slots, and one to 16 PCI slots (see Table 1-1). A standard ISA CPU may be installed in any ISA slot. For full use of the PCI and ISA buses, your CPU must include a PICMG-compliant PCI local bus extension connector installed in the ISA/PCI CPU slot. To overcome the PCI load limitations, many backplanes incorporate the DEC 21152 PCI-to-PCI bridge chip. This chip adds a secondary, independent PCI bus, which can increase overall performance in certain applications.

Configurations

Table 1-1 lists the ISA/PCI backplane configurations.

Table 1-1: ISA/PCI Backplane Configurations

Model Number	ISA Slots	ISA/PCI CPU Slot	PCI Slots	Notes
15005-02	2	1	2	
15008-02	3	1	4	One PCI slot on primary PCI bus, three on secondary.
14008-02	5	1	2	
15013-02	6	1	6	Two PCI slots on primary PCI bus, four on secondary.
15013-04	8	1	4	One PCI slot on primary PCI bus, three on secondary.
14013-10	10	1	2	
15016-02	8	4	4	Two ISA slots and one PCI slot per CPU.
14018-02	15	1	2	
15018-02	8	1	9	One PCI slot on primary PCI bus, four on secondary, four more on additional secondary bus.
15018-10	11	1	6	Two PCI slots on primary PCI bus, four on secondary.
15018-16	1	1	16	Four PCI slots on each of four secondary PCI buses.

The ISA/PCI backplanes feature a low-capacitance design that minimizes signal crosstalk and trace capacitance. This design improves signal edges and rise and fall times. Most backplanes also have a bank of LEDs to indicate the presence of power supply levels of the standard PC bus: ±5VDC, ±12VDC, and +3.3VDC. These LEDs provide a quick check of power supply operation without using a multimeter.

ICS Advent passive backplanes have been tested with a variety of plug-in CPU cards, from 8088 XT through Pentium and DEC Alpha systems. For applications involving option cards that are sensitive to bus impedance, termination SIPs are available as plug-ins for the ISA bus. Refer to Chapter 3 for more information.

Backplane Construction

ISA/PCI backplanes have four or six layers, depending on the model. The backplanes incorporate internal ground and power planes for RFI and EMI noise immunity and low-trace capacitance.

The four-layer boards include the 15005-02, 14008-02, 14013-10, 15016-02, and 04018-02. Signal traces, clock, and control signals are on the outer layers (1 and 4). Layer 2 is the ground plane, and layer 3 is the power plane.

The six-layer boards include the 15008-02, 15013-02, 15013-04, 15018-02, 15018-10, and 15018-16. Signal traces are on the outer layers (1 and 6) and the inner layers (3 and 4). The inner signal layers are used for clock and control signals. Layer 2 is the ground plane, and layer 5 is the power plane.

Input Power

One or more large electrolytic capacitors filter input power to reduce low-frequency line noise. The five input voltages have ceramic bypass filter capacitors of 0.01µF to improve noise immunity.

The exclusive ICS Advent Bus Power Check™ circuitry monitors the five supply voltages. An LED for each voltage which provides quick, visual verification. However, you may need to measure the power supply values during troubleshooting.

Note: Troubleshooting may require a load on the power supply. ICS Advent offers an optional ISA plug-in power supply load board that provides minimum loading requirements of 0.96A on +12VDC and 4A on +5VDC. Please mention Model 10273-01B when ordering.

Connectors

The five-, eight-, and 13-slot backplanes provide four six-pin connectors for power input. The 18-slot backplanes provide a single 16-pin connector. A variety of auxiliary power and sense connectors are also available for various chassis functions. Chapter 2 contains connector assignments for the ISA/PCI backplanes.

CAUTION!

Some video cards cause bus contention when placed in certain PCI slots. This causes fatal bus errors and potential damage due to overheating. Avoid this condition by placing your video card in Slot 2 for the 15013-02 backplane or Slot 1 on the 15008-02, 15018-02, and 15018-10 backplanes. Video cards that are PCI 2.1-compliant will not cause errors in a bridge chip environment.

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Chapter 2: Connectors and Dimensions

This chapter lists the connectors and shows the dimensions and major components of the ISA/PCI backplanes.

Five-Slot Backplane Model 15005-02 (Figure 2-1)

WARNING!

Do not exceed the current limitations listed in Table 2-1. To do so may cause a fire hazard.

Table 2-1: Model 15005-02 Total Current Limitations

Line	Limit
+3.3VDC	21A
+5VDC	29.4A
-5VDC	11.2A
+12VDC	11.2A
-12VDC	11.2A

P2: Drive Power Out Connector

4-pin single row, Amp 640457-4

1	+12VDC	3	GND
2	GND	4	+5VDC

P3: Drive Power Out Connector

4-pin single row, Amp 640457-4

1	+12VDC	3	GND
2	GND	4	+5VDC

P7: CPU Connector

8-pin single row, Amp 640457-8

1	SPKDATA	5	KBDCLK
2	N/C	6	N/C
3	KBDLOCK	7	GND
4	KBDDAT	8	RESET

P8: Power Supply Connector

6-pin single row, Adamtech PLHB-06TS

1	N/C	4	-12VDC
2	N/C	5	GND
3	+12VDC	6	GND

P9: Power Supply Connector

6-pin single row, Adamtech PLHB-06TS

1	GND	4	+5VDC
2	GND	5	+5VDC
3	-5VDC	6	+5VDC

Five-Slot Backplane (continued)

P10: 5 Volt Power Connector

Revision B of this board does not use P10. Revision C and above have P10 populated and connected as follows:

6-pin single row, Adamtech PLHB-06TS

1	+5VDC	4	GND
2	+5VDC	5	GND
3	+5VDC	6	GND

P11: 3.3 Volt Power Connector

6-pin single row, Adamtech PLHB-06TS

1	+3.3VDC	4	GND
2	+3.3VDC	5	GND
3	+3.3VDC	6	GND

P12: Front Panel I/O Connector

12-pin single row, Amp 1-640456-2

1	-12VDC	7	KBDCLK
2	+12VDC	8	-5VDC
3	SPKDATA	9	GND
4	+5VDC	10	RESET
5	KBDLOCK	11	GND
6	KBDDAT	12	+3.3VDC

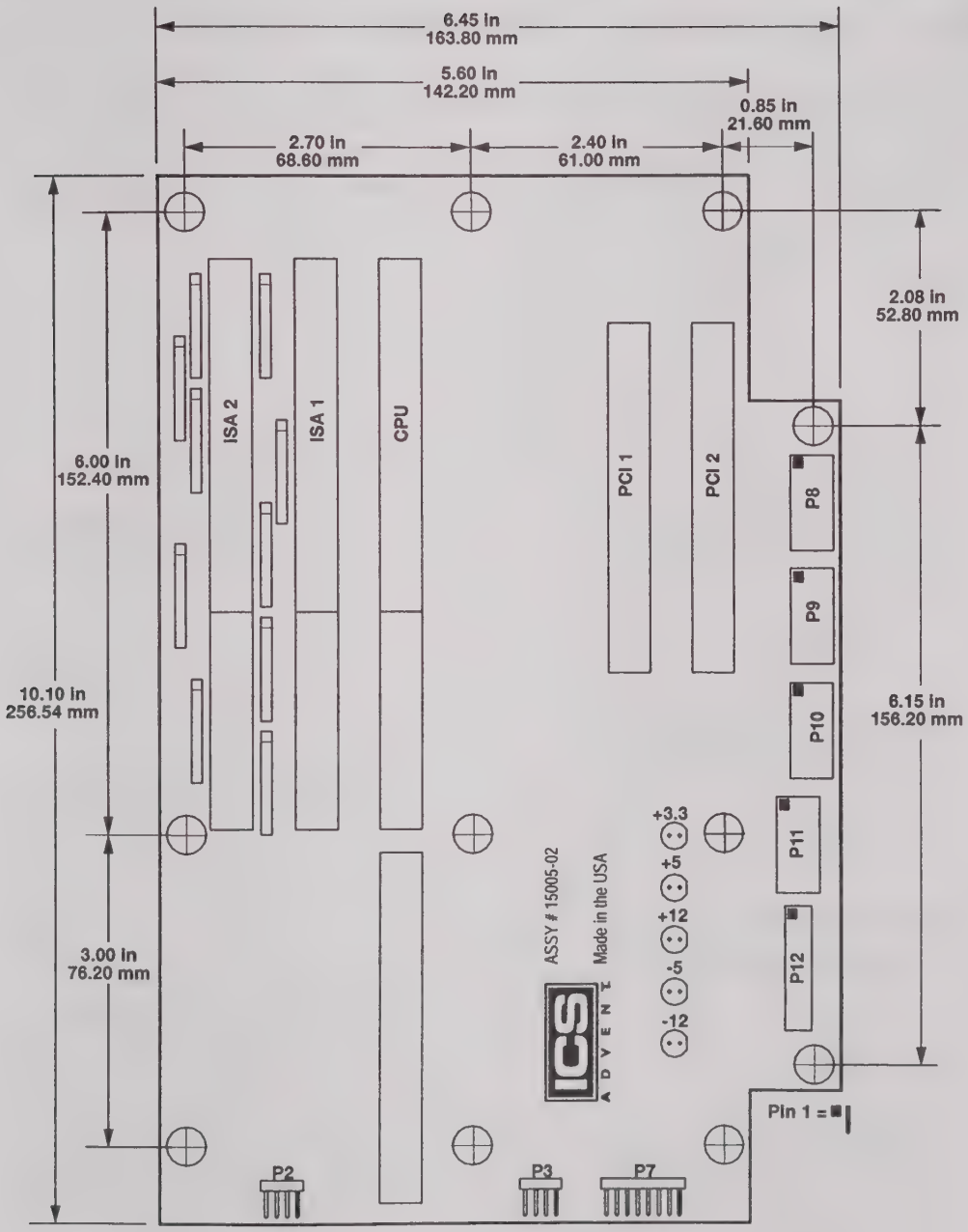

Figure 2-1: Five-Slot Backplane (15005-02)

Eight-Slot Backplanes
Models 14008-02, 15008-02 (Figures 2-2, 2-3)

WARNING!

Do not exceed the current limitations listed in Table 2-2. To do so may cause a fire hazard.

Table 2-2: Model 15008-02 and Model 114008-02 Total Current Limitations

Line	Limit
+3.3VDC	21A
+5VDC	29.4A
-5VDC	11.2A
+12VDC	11.2A
-12VDC	11.2A

P1: I/O Power Out Connector
3-pin single row, Amp 640457-3

1	+5VDC	3	GND
2	+12VDC		

P3: Drive Power Out Connector
4-pin single row, Amp 640457-4

1	+12VDC	3	GND
2	GND	4	+5VDC

P5: I/O Power Out Connector
2-pin single row, Amp 640457-2

1	+5VDC
2	GND

P7: CPU Connector
8-pin single row, Amp 640457-8

1	SPKDATA	5	KBDCLK
2	N/C	6	N/C
3	KBDLOCK	7	GND
4	KBDDAT	8	RESET

P8: Power Supply Connector
6-pin single row, Adamtech PLHB-06TS

1	N/C	4	-12VDC
2	N/C	5	GND
3	+12VDC	6	GND

P9: Power Supply Connector
6-pin single row, Adamtech PLHB-06TS

1	GND	4	+5VDC
2	GND	5	+5VDC
3	-5VDC	6	+5VDC

P10: 5 Volt Power Connector
6-pin single row, Adamtech PLHB-06TS

1	+5VDC	4	GND
2	+5VDC	5	GND
3	+5VDC	6	GND

P11: 3.3 Volt Power Connector

6-pin single row, Adamtech PLHB-06TS

1	+3.3VDC	4	GND
2	+3.3VDC	5	GND
3	+3.3VDC	6	GND

P12: Front Panel I/O Connector

12-pin single row, Amp 1-640457-2

1	-12VDC	7	KBDCLK
2	+12VDC	8	-5VDC
3	SPKDATA	9	GND
4	+5VDC	10	RESET
5	KBDLOCK	11	GND
6	KBDDAT	12	+3.3VDC

Eight-Slot Backplanes (continued)

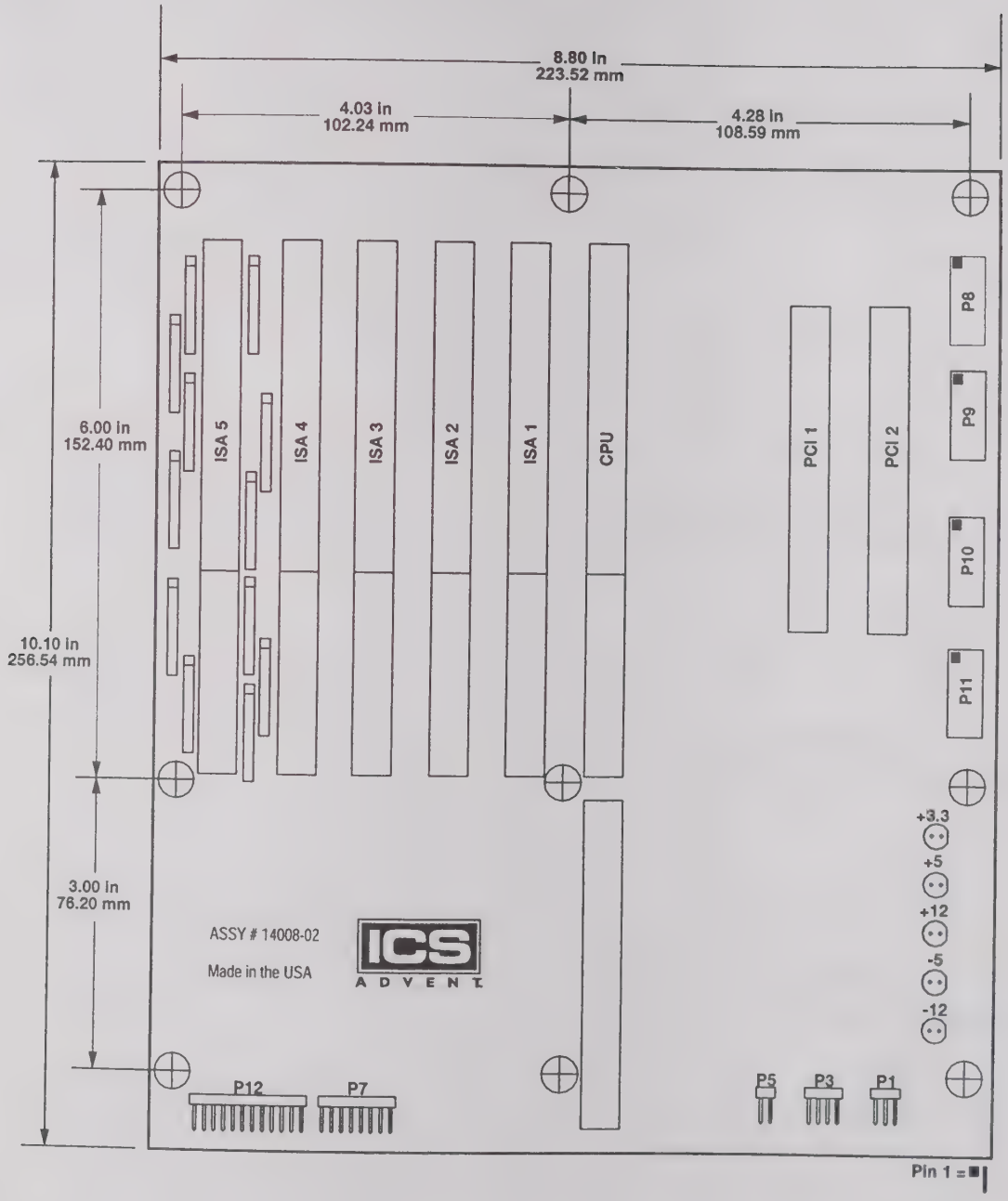

Figure 2-2: Eight-Slot Backplane (14008-02)

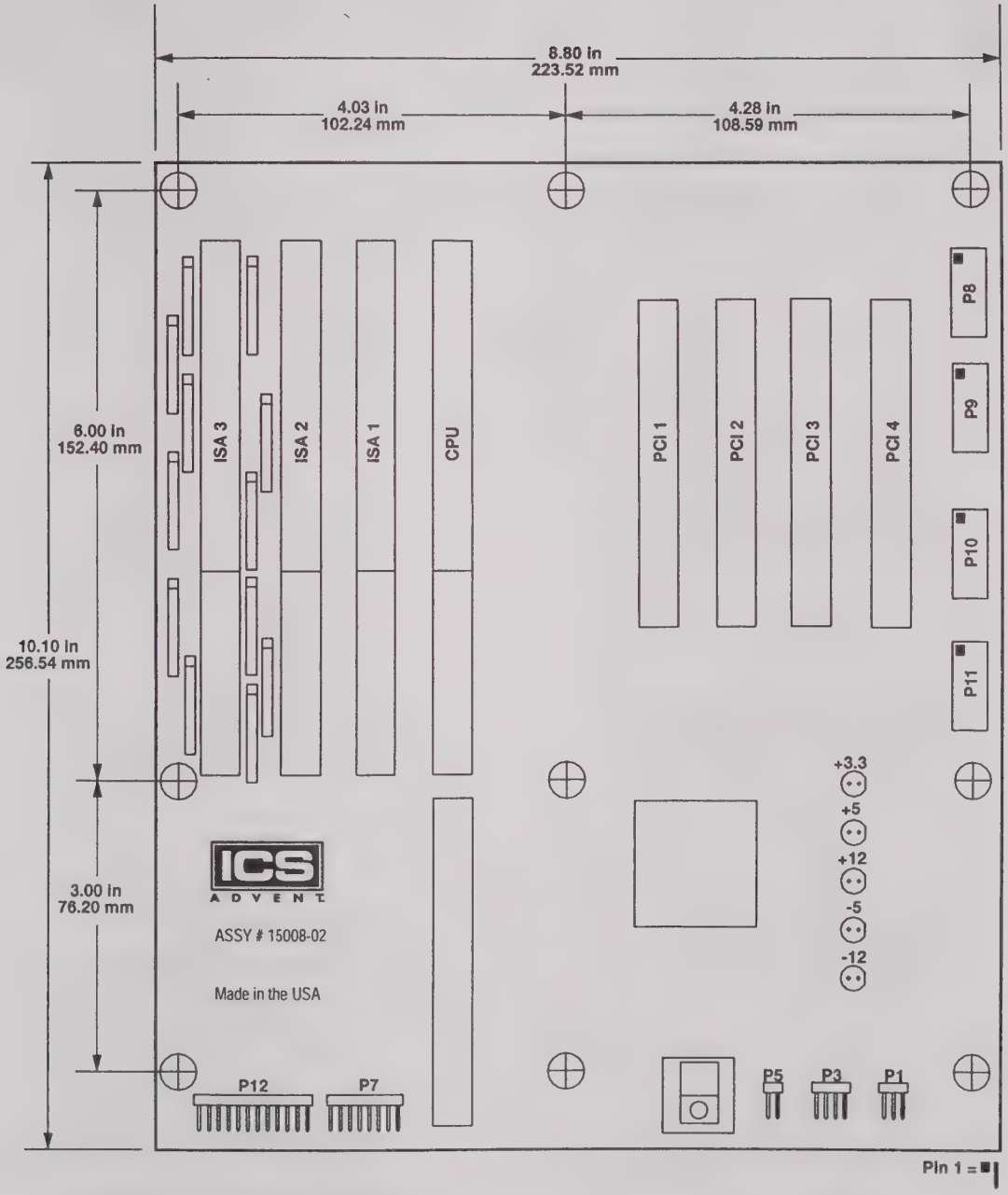

Figure 2-3: Eight-Slot Backplane (15008-02)

Thirteen-Slot Backplanes
Models 14013-10, 15013-02, 15013-04 (Figures 2-4, 2-5, 2-6)

WARNING!

Do not exceed the current limitations listed in Table 2-3. To do so may cause a fire hazard.

Table 2-3: Models 14013-10, 15013-02, 15013-04 Total Current Limitations

Line	Limit
+3.3VDC	21A
+5VDC	29.4A
-5VDC	11.2A
+12VDC	11.2A
-12VDC	11.2A

P1: I/O Power Out Connector
3-pin single row, Amp 640457-3

1	+5VDC	3	GND
2	+12VDC		

P2: Drive Power Out Connector
4-pin single row, Amp 640389-4

1	+12VDC	3	GND
2	GND	4	+5VDC

P3: Drive Power Out Connector
4-pin single row, Amp 640457-4

1	+12VDC	3	GND
2	GND	4	+5VDC

P4: I/O Power Out Connector
3-pin single row, Amp 640389-3

1	+5VDC	3	GND
2	+12VDC		

P5: Remote Sense Connector
2-pin single row, Amp 640457-2

1	+5VDC
2	GND

P6: I/O Power Out Connector
3-pin single row, Amp 640389-3

1	+5VDC	3	GND
2	+12VDC		

P7: CPU Connector
8-pin single row, Amp 640457-8

1	SPKDATA	5	KBDCLK
2	N/C	6	N/C
3	KBDLOCK	7	GND
4	KBDDAT	8	RESET

P8: Power Supply Connector
6-pin single row, Adamtech PLHB-06TS

1	N/C	4	-12VDC
2	N/C	5	GND
3	+12VDC	6	GND

P9: Power Supply Connector

6-pin single row, Adamtech PLHB-06TS

1	GND	4	+5VDC
2	GND	5	+5VDC
3	-5VDC	6	+5VDC

P10: 5 Volt Power Connector

6-pin single row, Adamtech PLHB-06TS

1	+5VDC	4	GND
2	+5VDC	5	GND
3	+5VDC	6	GND

P11: 3.3 Volt Power Connector

6-pin single row, Adamtech PLHB-06TS

1	+3.3VDC	4	GND
2	+3.3VDC	5	GND
3	+3.3VDC	6	GND

P12: Front Panel I/O Connector

12-pin single row, Amp 1-640456-2

1	-12VDC	7	KBDCLK
2	+12VDC	8	-5VDC
3	SPKDATA	9	GND
4	+5VDC	10	RESET
5	KBDLOCK	11	GND
6	KBDDAT	12	+3.3VDC

Thirteen-Slot Backplanes (continued)

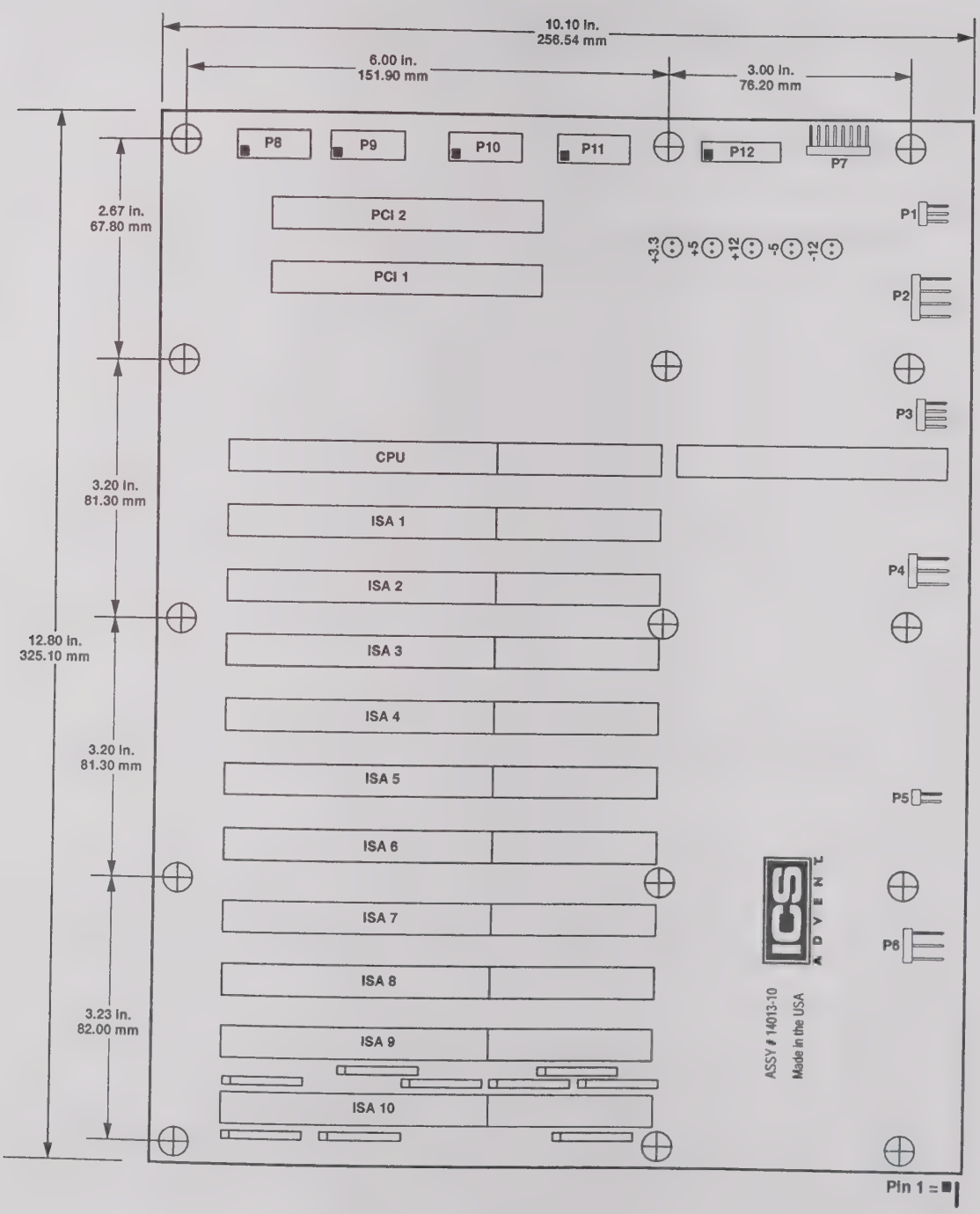

Figure 2-4: Thirteen-Slot Backplane (14013-10)

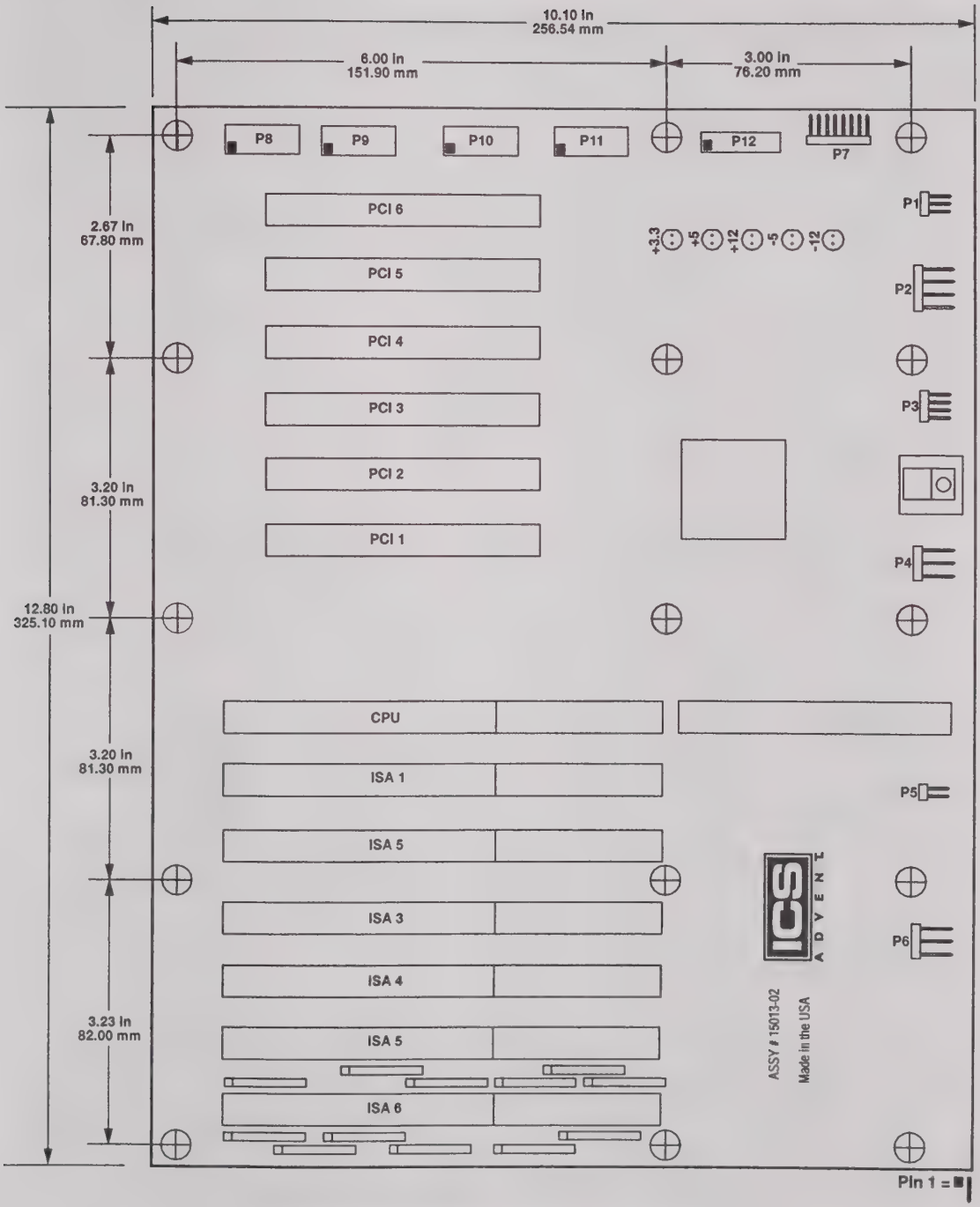

Figure 2-5: Thirteen-Slot Backplane (15013-02)

Thirteen-Slot Backplanes (continued)

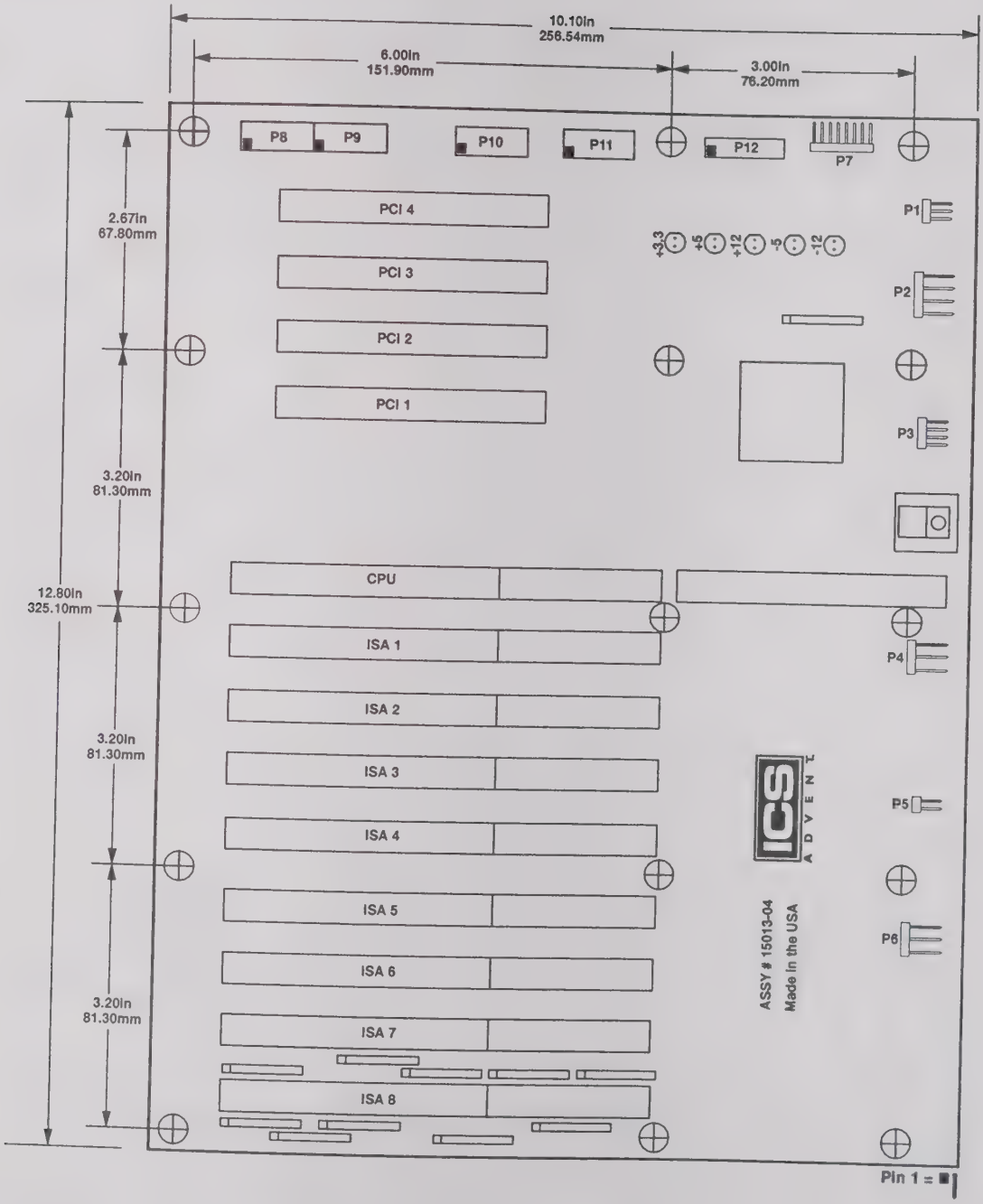

Figure 2-6: Thirteen-Slot Backplane (15013-04)

Sixteen-Slot Backplane Model 15016-02 (Figure 2-7)

WARNING!

Do not exceed the current limitations listed in Table 2-4. To do so may cause a fire hazard.

Table 2-4: Models 15016-02 Total Current Limitations

Line	Limit
+3.3VDC	21A
+5VDC	34.3A
-5VDC	11.2A
+12VDC	11.2A
-12VDC	11.2A

P2: Front Panel I/O Connector
12-pin single row, Amp 1-640457-2

1	-12VDC	7	NC
2	+12VDC	8	-5VDC
3	NC	9	GND
4	+5VDC	10	NC
5	NC	11	GND
6	NC	12	+3.3VDC

P3: Remote Sense Connector
2-pin single row, Amp 640457-2

1	+5VDC
2	GND

P8: I/O Power Out Connector
3-pin single row, Amp 640389-3

1	+5VDC	3	GND
2	+12VDC		

P9: Power Supply Connector
16-pin single row, Amp 1-640389-6

1	N/C	9	GND
2	N/C	10	GND
3	+12VDC	11	-5VDC
4	-12VDC	12	+5VDC
5	GND	13	+5VDC
6	GND	14	+5VDC
7	GND	15	+5VDC
8	GND	16	+5VDC

P11: I/O Power Out Connector
3-pin single row, Amp 640389-3

1	+5VDC	3	GND
2	+12VDC		

P13: 3.3 Volt Power Connector
6-pin single row, Amp 640389-6

1	+3.3VDC	4	GND
2	+3.3VDC	5	GND
3	+3.3VDC	6	GND

Sixteen-Slot Backplanes (continued)

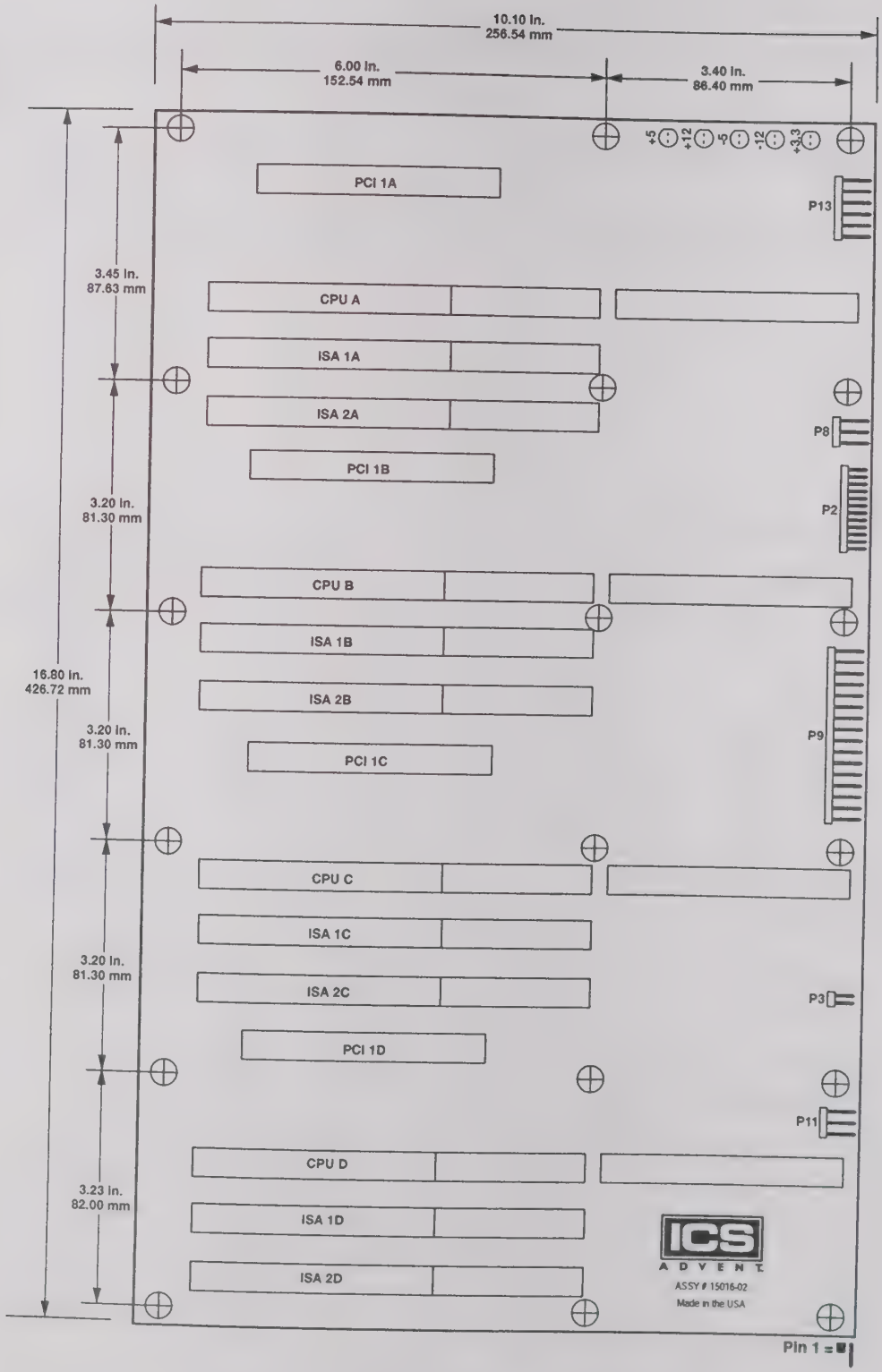

Figure 2-7: Sixteen-Slot Backplane (15016-02)

Eighteen-Slot Backplanes Models 14018-02, 15018-02, 15018-10, 15018-16 (Figures 2-8 through 2-11)

WARNING!

Do not exceed the current limitations listed in Table 2-5. To do so may cause a fire hazard.

Table 2-5: Models 14018-02, 15018-02, 15018-10, 15018-16 Total Current Limitations

Line	Limit
+3.3VDC	21A
+5VDC	34.3A
-5VDC	14A
+12VDC	21A
-12VDC	14A

P1: Remote Sense Connector
2-pin single row, Amp 640457-2

1	+5VDC
2	GND

P2: Connection to Front Panel I/O
12-pin single row, Amp 1-640457-2

1	-12VDC	7	KBDCLK
2	+12VDC	8	-5VDC
3	SPKDATA	9	GND
4	+5VDC	10	RESET
5	KBDLOCK	11	GND
6	KBDDAT	12	+3.3VDC

P3: Remote Sense Connector
2-pin single row, Amp 640457-2

1	+5VDC
2	GND

P4: I/O Power Out Connector
3-pin single row, Amp 640457-3

1	+5VDC	3	GND
2	+12VDC		

P5: Auxilary CPU Connector
8-pin single row, Amp 640457-8

1	SPKDATA	5	KBDCLK
2	N/C	6	N/C
3	KBDLOCK	7	GND
4	KBDDAT	8	RESET

P6: Drive Power Out Connector
4 pin single row, Amp 640389-4

1	+12VDC	3	GND
2	GND	4	+5VDC

P7: Drive Power Out Connector
4-pin single row, Amp 640389-4

1	+12VDC	3	GND
2	GND	4	+5VDC

Eighteen-Slot Backplanes (continued)

P8: I/O Power Out Connector

3-pin single row, Amp 640389-3

1	+5VDC	3	GND
2	+12VDC		

P9: Power Supply Connector

16-pin single row, Amp 1-640389-6

1	N/C	9	GND
2	N/C	10	GND
3	+12VDC	11	-5V DC
4	-12VDC	12	+5V DC
5	GND	13	+5VDC
6	GND	14	+5VDC
7	GND	15	+5VDC
8	GND	16	+5V DC

P10: Power Supply Connector

6-pin single row, Amp 640389-6

1	-12VDC	4	-5VDC
2	GND	5	+12VDC
3	GND	6	+5VDC

P11: I/O Power Out Connector

3-pin single row, Amp 640389-3

1	+5VDC	3	GND
2	+12VDC		

P12: 5 Volt Power Connector

6-pin single row, Amp 640389-6

1	+5VDC	4	GND
2	+5VDC	5	GND
3	+5VDC	6	GND

P13: 3.3 Volt Power Connector

6-pin single row, Amp 640445-6

1	+3.3VDC	4	GND
2	+3.3VDC	5	GND
3	+3.3VDC	6	GND

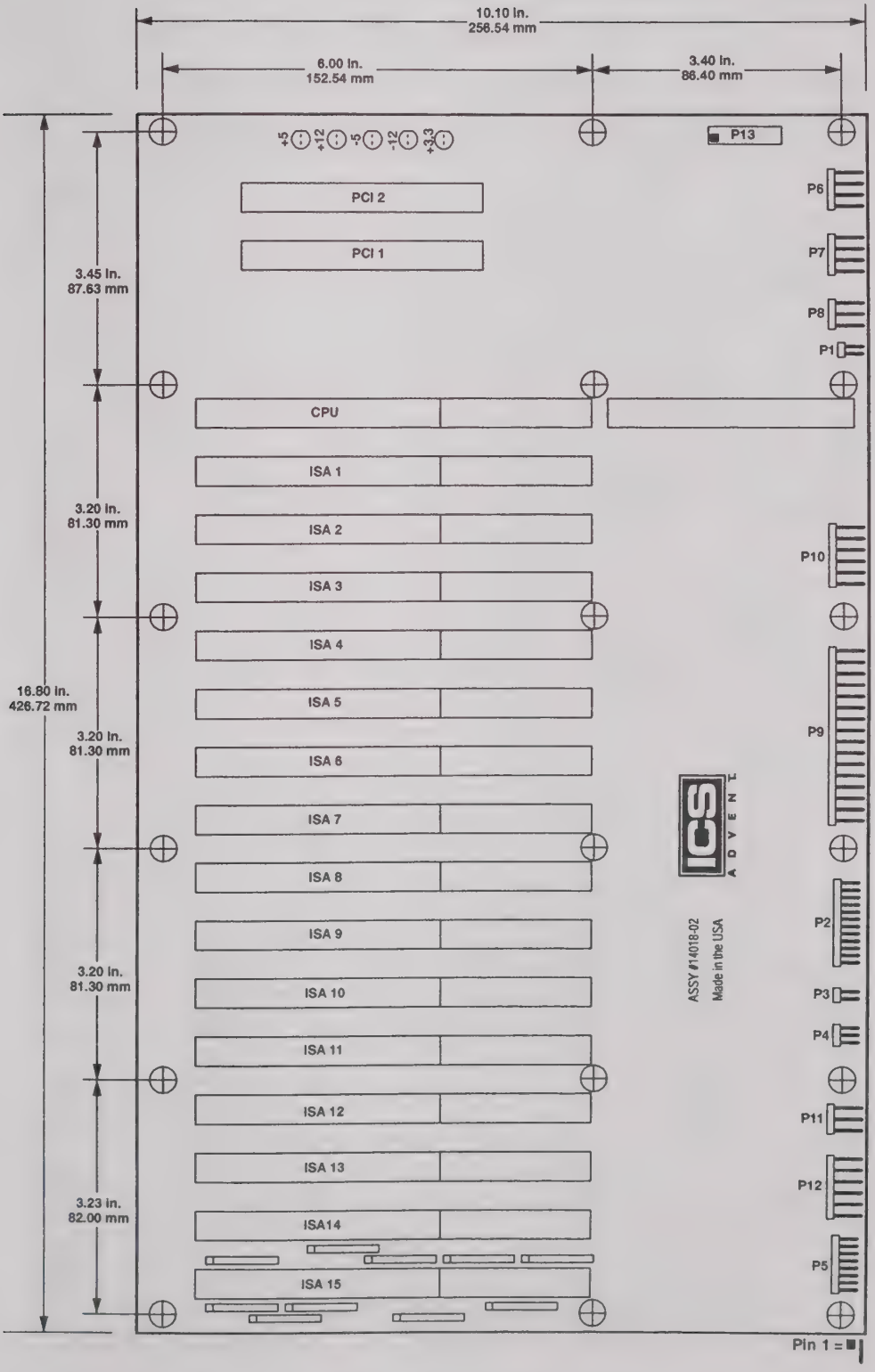

Figure 2-8: Eighteen-Slot Backplane (14018-02)

Eighteen-Slot Backplanes (continued)

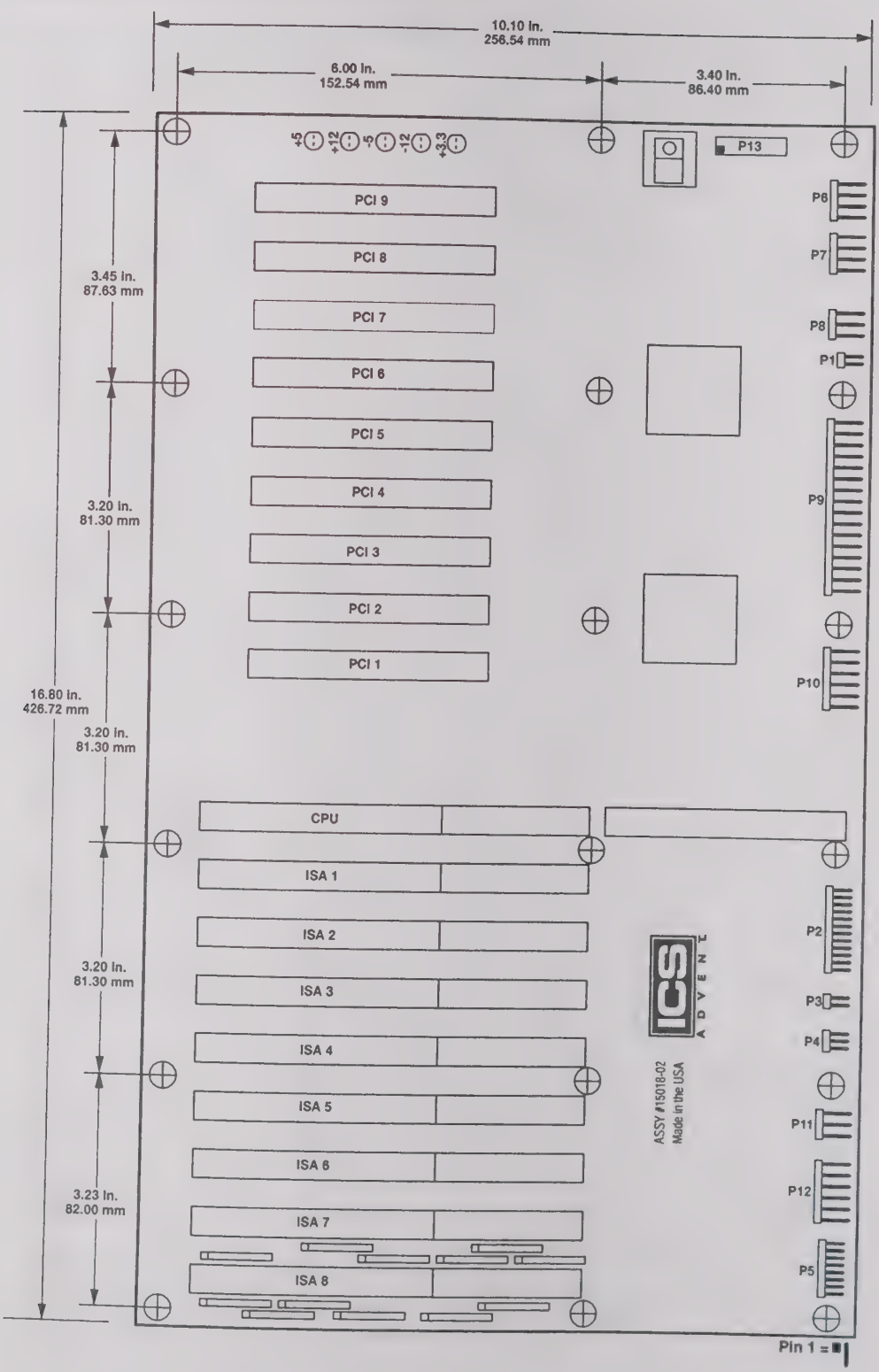

Figure 2-9: Eighteen-Slot Backplane (15018-02)

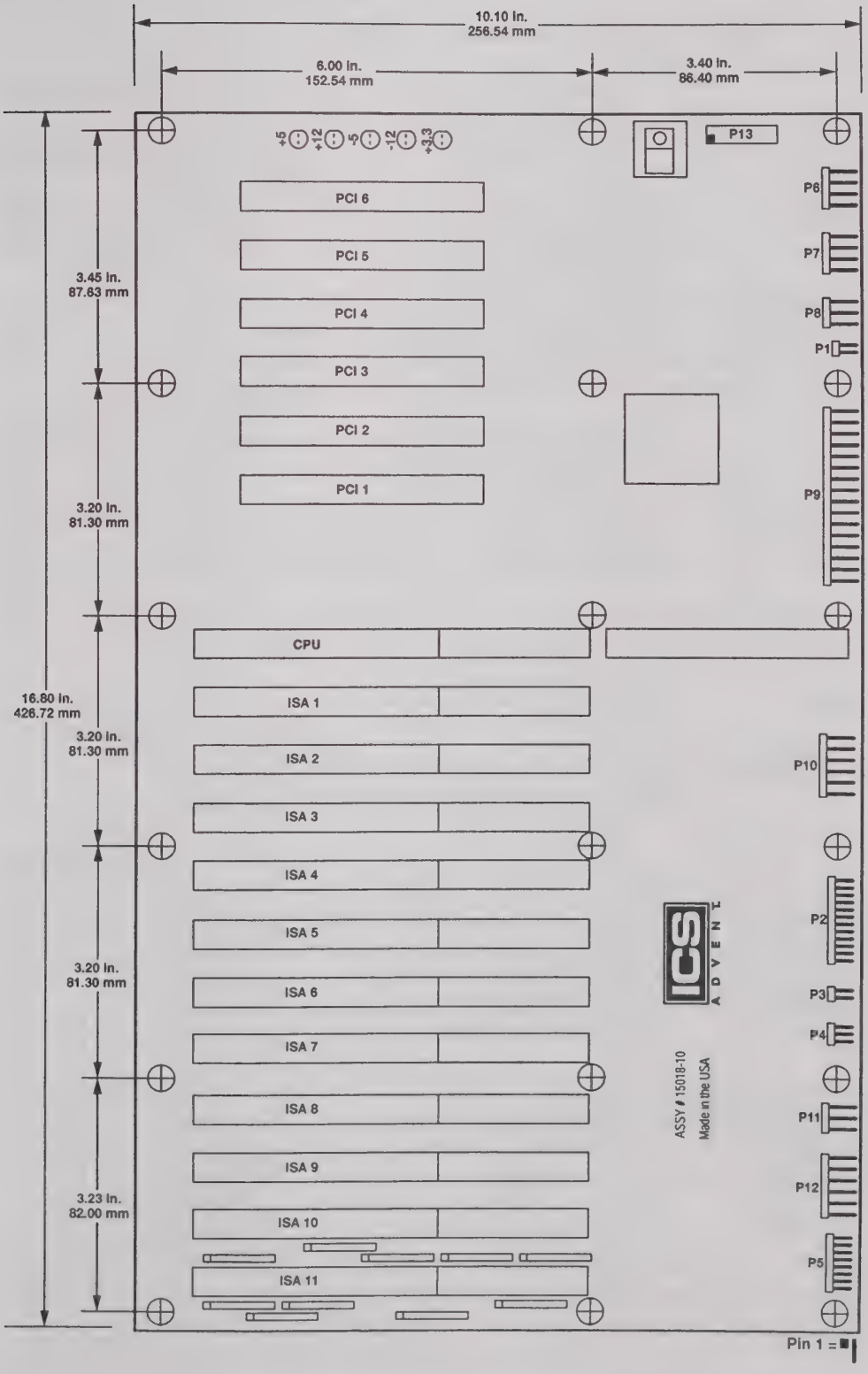

Figure 2-10: Eighteen-Slot Backplane (15018-10)

Eighteen-Slot Backplanes (continued)

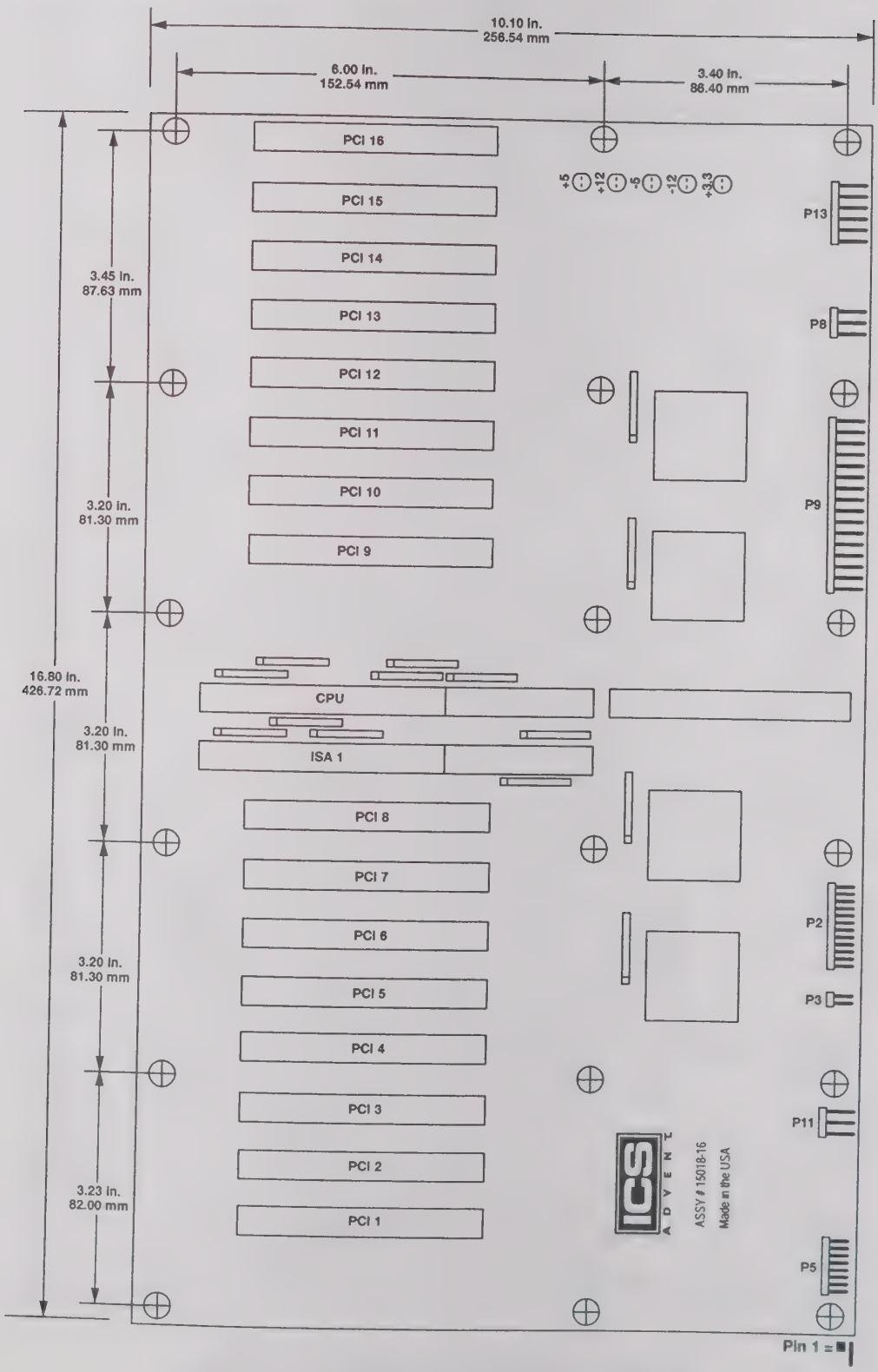

Figure 2-11: Eighteen-Slot Backplane (15018-16)

Chapter 3: ISA Bus Overview

This chapter describes ISA bus signals and their pin assignments.

ISA Bus Signal Descriptions

All signal lines are TTL-compatible. A # symbol at the end of a signal name indicates that the signal is active *low*. When the # symbol is absent, the signal is active *high*.

AEN — Address ENable (AEN) releases the microprocessor and other devices from the I/O channel to allow direct memory access (DMA) transfers. When this line is active, the DMA controller has control of the address bus, the data-bus Read command lines (memory and I/O), and the Write command lines (memory and I/O).

BALE — Address Latch Enable (BALE) is provided by the bus controller and is used on the system board to latch valid addresses and memory decodes from the microprocessor. BALE is available to the I/O channel to indicate a valid microprocessor or DMA address (when used with AEN). Microprocessor addresses SA[19..0] are latched with the falling edge of BALE. During DMA cycles, BALE is forced high.

CLK — The system clock (CLK) has a 50 percent duty cycle. This signal should only be used for synchronization. Do not use the signal in applications that require a fixed frequency.

DACK[7..5]#, DACK[3..0]# — Direct-memory-access ACKnowledge signals (DACK[7..5]# and DACK[3..0]#) acknowledge DMA requests DRQ[7..5] and DRQ[3..0].

DRQ[7..5], DRQ[3..0] — Direct-memory-access ReQuests (DRQ[7..5] and DRQ[3..0]) are asynchronous channel requests. Peripheral devices and the I/O channel microprocessors use these signals to gain DMA service or control of the system. DRQ0 has the highest priority; DRQ7, the lowest. To generate a request, bring a DRQ level active and hold it high until the corresponding DACK line goes active. DRQ[3..0] performs 8-bit DMA transfers and DRQ[7..5] performs 16-bit transfers.

I/O CHRDY — I/O CHannel ReaDY (I/OCHRDY) is pulled low by memory or I/O devices to lengthen memory or I/O cycles. Any slow device using this line should drive it low immediately upon detecting its valid address and a Read or Write command. Machine cycles are extended by an integral number of clock cycles. Hold this low for no more than 2.5 µsec.

IOCHK# — I/O Channel CHecK provides the system board with parity information about memory or devices on the I/O channel. When this signal is active, it indicates an uncorrectable system error.

IOCS16# I/O 16 Chip Select signals the system board that the present data transfer is a 16-bit, 1-wait-state, I/O cycle. The signal is derived from an address decode. IOCS16# is active low and should be driven with an open collector or tri-state driver capable of sinking 20mA.

IOR# I/O Read instructs an I/O device to read the contents of the data bus. The signal may be driven by a microprocessor or DMA controller in the system or resident on the I/O channel.

IOW# I/O Write instructs an I/O device to drive its contents onto the data bus. The signal may be driven by any microprocessor or DMA controller in the system.

IRQ[15,14], IRQ[12..9], IRQ[7..3]

Interrupt ReQuests signal the microprocessor that an I/O device needs attention. IRQ[15..14] and IRQ[12..9] have the higher priority (IRQ9 is the highest). IRQ[7..3] have the lower priority (IRQ7 is the lowest). IRQ lines must be held high until the microprocessor acknowledges the request (through an interrupt service routine).

LA[23..17] These signals (unLAtched) address memory and I/O devices within the system, providing up to 16MB of addressability. LA[23..17] are unlatched during microprocessor cycles and therefore do not stay valid for the whole cycle. They generate memory decodes for 1-wait-state cycles. These signals are valid when BALE is high and should be latched by I/O adapters on the falling edge of BALE. The signals also may be driven by other microprocessors or DMA controllers that reside on the I/O channel.

Master# Master# is used with a DRQ line to gain control of the system. A processor or DMA controller on the I/O channel may issue a DRQ to a DMA channel in cascade mode and receive a DACK#. Upon receiving the DACK#, an I/O microprocessor may pull Master# low, which will allow it to control the system address, data, and control lines (a condition known as tri-state). After Master# is low, the I/O microprocessor must wait one system clock period before driving the address and data lines, and two clock periods before issuing a Read or Write command. If this signal is held low for more than 15 µsec, system memory may be lost because it is not refreshed in the low state.

MEMCS16# MEMory16# Chip Select signals the system board if the present data transfer is a 1-wait-state, 16-bit, memory cycle. The signal is derived from an address decode LA[23..17]. Drive MEMCS16# with an open collector or tri-state driver capable of sinking 20mA.

0WS# The Zero Wait State (0WS#) signal tells the microprocessor that it can complete the present bus cycle without inserting any additional wait cycles. To run a memory cycle to a 16-bit device without wait cycles, derive the 0WS# from an address decode gated with a Read or Write command. To run a memory cycle to an 8-bit device with a minimum of 2 wait states, first gate the address decode with a Read or Write command, then drive 0WS# active on the falling edge of the system clock. Drive 0WS# with an open collector or tri-state driver capable of sinking 20mA.

OSC — Oscillator (OSC) is a high-speed clock with a 70-nsec period (14.31818 MHz). This signal is not synchronous with the system clock. It has a 50 percent duty cycle.

REFRESH# — The REFRESH# signal indicates a refresh cycle and can be driven by a microprocessor on the I/O channel.

RESET — RESET either resets or initializes system logic at power-up or during a low line-voltage outage.

SA[19..0] — System Address bits (SA[19..0)] address memory and I/O devices. These twenty address lines, in addition to LA[23..17], allow access of up to 16MB of memory. SA[19..0] are gated on the system bus when BALE is high and are latched in the falling edge of BALE. These signals are generated by the microprocessors or DMA controller. They also may be driven by other microprocessors or DMA controllers that reside in the I/O channel.

SBHE# — System Bus High Enable (SBHE#) indicates a transfer of data on the upper byte of the data bus, SD[15..8]. 16-bit devices use SBHE# to condition data bus buffers tied to SD[15..8].

SD[15..0] — System Data (SD[15..0]) signals provide bus bits 15 through 0 for the microprocessor, memory, and I/O devices. SD15 is the most-significant bit; SD0, the least. All 8-bit devices on the I/O channel use SD[7..0] for communications to the microprocessor. The 16-bit devices use SD[15..0]. To support 8-bit devices, the data on SD[15..8] will be gated to SD[7..0] during 8-bit transfers. Transfers from 16-bit to 8-bit devices will be converted to two 8-bit transfers.

SMEMR#, MEMR#

These MEMory Read signals instruct memory devices to drive data onto the data bus. SMEMR# is active only when the memory decode is within the low 1MB of memory space. MEMR# is active on all memory read cycles. MEMR# may be driven by any microprocessor or DMA controller in the system. To drive MEMR#, the address lines must be valid on the bus for one system clock period. SMEMR# is driven by MEMR# and the decode of the low 1MB of memory.

SMEMW#, MEMW#

These MEMory Write signals instruct memory devices to store data present on the data bus. SMEMW# is active only when the memory decode is within the low 1MB of the memory space. MEMW# is active on all memory write cycles. MEMW# may be driven by any microprocessor or DMA controller in the system. To drive MEMW#, the address lines must be valid on the bus for one system clock period.

T/C — Terminal Count (T/C) provides a pulse when the terminal count for any DMA channel is reached.

Bus Pin and Resistor Assignments

Tables 3-1 through 3-4 define the ISA bus pin and resistor assignments. (The 15016-02 has *no* SIP resistors.) Figure 3-1 shows the bus orientation, noting pin 1 on each of the four sides. The A and B sides are common to both XT (8-bit) and AT (16-bit) products. The C and D sides are used in AT-compatible systems.

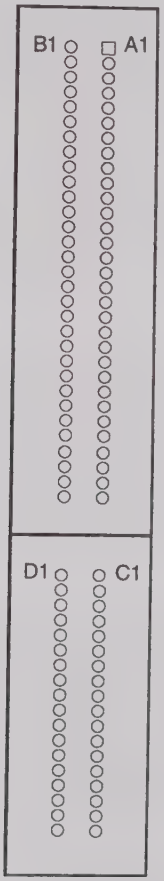

Figure 3-1: ISA Bus Pinouts

Table 3-1: XT (8-Bit) Bus Pin Assignments

XT (8-Bit) Bus Side A		
Pin	RN Pin	Description
1	12-2	I/OCHK#
2	11-2	SD7
3	11-3	SD6
4	11-4	SD5
5	11-5	SD4
6	11-6	SD3
7	11-7	SD2
8	11-8	SD1
9	11-9	SD0
10	NC	I/OCHRDY
11	12-9	AEN
12	10-6	SA19
13	10-7	SA18
14	10-8	SA17
15	10-9	SA16
16	8-2	SA15
17	8-3	SA14
18	8-4	SA13
19	8-5	SA12
20	8-6	SA11
21	8-7	SA10
22	8-8	SA9
23	8-9	SA8
24	7-2	SA7
25	7-3	SA6
26	7-4	SA5
27	7-5	SA4
28	7-6	SA3
29	7-7	SA2
30	7-8	SA1
31	7-9	SA0

XT (8-Bit) Bus Side		
Pin	RN Pin	Description
1	NC	Ground
2	4.7K	Reset
3	NC	+5 Volts
4	NC	IRQ2 or 9
5	NC	-5 Volts
6	NC	DRQ2
7	NC	-12 Volts
8	12-7	0WS#
9	NC	+12 Volts
10	NC	Ground
11	9-2	SMEMW#
12	9-3	SMEMR#
13	9-4	IOW#
14	9-5	IOR#
15	9-6	DACK3#
16	NC	DRQ3
17	9-7	DACK1#
18	NC	DRQ1
19	9-8	REFRESH#
20	9-9	CLK
21	NC	IRQ7
22	NC	IRQ6
23	NC	IRQ5
24	NC	IRQ4
25	NC	IRQ3
26	6-2	DACK2#
27	6-3	T/C
28	6-4	BALE
29	NC	+5Volts
30	6-5	OSC
31	NC	Ground

Note: Pin B4 is IRQ2 for an XT but IRQ9 for an AT. The IRQ9 signal is redirected as IRQ2 in an AT. Pin B19 (REFRESH#) is DACK0# on an XT system.

Table 3-2: AT (16-Bit) Bus Extension Pin Assignments

AT (16-Bit) Side C		
Pin	RN Pin	Description
1	6-7	SBHE#
2	5-3	LA23
3	5-4	LA22
4	5-5	LA21
5	5-6	LA20
6	5-7	LA19
7	5-8	LA18
8	5-9	LA17
9	4-4	MEMR#
10	4-6	MEMW#
11	3-2	SD08
12	3-3	SD09
13	3-4	SD10
14	3-5	SD11
15	3-6	SD12
16	3-7	SD13
17	3-8	SD14
18	3-9	SD15

AT (16-Bit) Side D		
Pin	RN Pin	Description
1	6-8	MEMCS16#
2	6-9	I/OCS16#
3	NC	IRQ10
4	NC	IRQ11
5	NC	IRQ12
6	NC	IRQ15
7	NC	IRQ14
8	4-2	DACK0#
9	NC	DRQ0#
10	4-5	DACK5#
11	NC	DRQ5
12	4-7	DACK6#
13	NC	DRQ6#
14	4-8	DACK7#
15	NC	DRQ7
16	NC	5VDC
17	4-9	MASTER#
18	NC	GROUND

Table 3-3: Bus Signals Sorted by SIP Resistors
ISA/PCI backplanes except 15016-02 and 15018-16

RN Pin	Side	Pin	Description
3-1			+5V
3-2	C	11	SD08
3-3	C	12	SD09
3-4	C	13	SD10
3-5	C	14	SD11
3-6	C	15	SD12
3-7	C	16	SD13
3-8	C	17	SD14
3-9	C	18	SD15
3-10			GND
4-1			+5V
4-2	D	8	DACK0#
4-3			NC
4-4	C	9	MEMR#
4-5	D	10	DACK5#
4-6	C	10	MEMW#
4-7	D	12	DACK6#
4-8	D	14	DACK7#
4-9	D	17	MASTER#
4-10			GND
5-1			+5V
5-2			NC
5-3	C	2	LA23
5-4	C	3	LA22
5-5	C	4	LA21
5-6	C	5	LA20
5-7	C	6	LA19
5-8	C	7	LA18
5-9	C	8	LA17
5-10			GND

RN Pin	Side	Pin	Description
6-1			+5V
6-2	B	26	DACK2#
6-3	B	27	T-C
6-4	B	28	BALE
6-5	B	30	OSC
6-6			NC
6-7	C	1	SBHE#
6-8	D	1	MEMCS16#
6-9	D	2	I/O16#
6-10			GND
7-1			+5V
7-2	A	24	SA7
7-3	A	25	SA6
7-4	A	26	SA5
7-5	A	27	SA4
7-6	A	28	SA3
7-7	A	29	SA2
7-8	A	30	SA1
7-9	A	31	SA0
7-10			GND
8-1			+5V
8-2	A	16	SA15
8-3	A	17	SA14
8-4	A	18	SA13
8-5	A	19	SA12
8-6	A	20	SA11
8-7	A	21	SA10
8-8	A	22	SA9
8-9	A	23	SA8
8-10			GND

Table 3-3: Bus Signals Sorted by SIP Resistors (continued)
ISA/PCI backplanes except 15016-02 and 15018-16

RN Pin	Side	Pin	Description
9-1			+5V
9-2	B	11	SMEMW#
9-3	B	12	SMEMR#
9-4	B	13	IOW#
9-5	B	14	IOR#
9-6	B	15	DACK3#
9-7	B	17	DACK1#
9-8	B	19	REFRESH#
9-9	B	20	CLK
9-10			GND
10-1			+5V
10-2			NC
10-3			NC
10-4			NC
10-5			NC
10-6	A	12	SA19
10-7	A	13	SA18
10-8	A	14	SA17
10-9	A	15	SA16
10-10			GND

RN Pin	Side	Pin	Description
11-1			+5V
11-2	A	2	SD7
11-3	A	3	SD6
11-4	A	4	SD5
11-5	A	5	SD4
11-6	A	6	SD3
11-7	A	7	SD2
11-8	A	8	SD1
11-9	A	9	SD0
11-10			GND
12-1			+5V
12-2	A	1	I/OCHK#
12-3			NC
12-4			NC
12-5			NC
12-6			NC
12-7	B	8	0WS#
12-8			NC
12-9	A	11	AEN
12-10			GND

Table 3-4: Bus Signals Sorted by SIP Resistors on 15018-16

RN Pin	Side	Pin	Description
5-1			+5V
5-2	C	11	SD08
5-3	C	12	SD09
5-4	C	13	SD10
3-5	C	14	SD11
5-6	C	15	SD12
5-7	C	16	SD13
5-8	C	17	SD14
5-9	C	18	SD15
5-10			GND
6-1			+5V
6-2	D	8	DACK0#
6-3			NC
6-4	C	9	MEMR#
6-5	D	10	DACK5#
6-6	C	10	MEMW#
6-7	D	12	DACK6#
6-8	D	14	DACK7#
6-9	D	17	MASTER#
6-10			GND
7-1			+5V
7-2			
7-3	C	2	LA23
7-4	C	3	LA22
7-5	C	4	LA21
7-6	C	5	LA20
7-7	C	6	LA19
7-8	C	7	LA18
7-9	C	8	LA17
7-10			GND

RN Pin	Side	Pin	Description
8-1			+5V
8-2	B	26	DACK2#
8-3	B	27	T-C
8-4	B	28	BALE
8-5	B	30	OSC
8-6			NC
8-7	C	1	SBHE#
8-8	D	1	MEMCS16#
8-9	D	2	I/O16#
8-10			GND
9-1			+5V
9-2	A	24	SA7
9-3	A	25	SA6
9-4	A	26	SA5
9-5	A	27	SA4
9-6	A	28	SA3
9-7	A	29	SA2
9-8	A	30	SA1
9-9	A	31	SA0
9-10			GND
10-1			+5V
10-2	A	16	SA15
10-3	A	17	SA14
10-4	A	18	SA13
10-5	A	19	SA12
10-6	A	20	SA11
10-7	A	21	SA10
10-8	A	22	SA9
10-9	A	23	SA8
10-10			GND

Table 3-4: Bus Signals Sorted by SIP Resistors on 15018-16 (continued)

RN Pin	Side	Pin	Description
11-1			+5V
11-2	B	11	SMEMW#
11-3	B	12	SMEMR#
11-4	B	13	IOW#
11-5	B	14	IOR#
11-6	B	15	DACK3#
11-7	B	17	DACK1#
11-8	B	19	REFRESH#
11-9	B	20	CLK
11-10			GND
12-1			+5V
12-2			NC
12-3			NC
12-4			NC
12-5			NC
12-6	A	12	SA19
12-7	A	13	SA18
12-8	A	14	SA17
12-9	A	15	SA16
12-10			GND

RN Pin	Side	Pin	Description
13-1			+5V
13-2	A	1	I/OCHK#
13-3			NC
13-4			NC
13-5			NC
13-6			NC
13-7	B	8	0WS#
13-8			NC
13-9	A	11	AEN
13-10			GND
14-1			+5V
14-2	A	2	SD7
14-3	A	3	SD6
14-4	A	4	SD5
14-5	A	5	SD4
14-6	A	6	SD3
14-7	A	7	SD2
14-8	A	8	SD1
14-9	A	9	SD0
14-10			GND

ISA Bus Termination

Termination provides an impedance mismatch at the end of the bus to prevent signal reflections. Without termination, signals reach the end of the bus and reflect back. In extreme cases, the reflected signals can interfere with real bus information, leading to spurious operation or lockups. A terminated bus also reduces signal noise and rise and fall times.

As bus lengths and speeds increase, termination may become essential. Applications most likely to be affected include telephony and those with many I/O boards drawing high current values off the +12V or -12V power connections. However, ICS Advent backplanes have supported 166MHz systems without bus termination and without problem.

The benefits of termination depend on your CPU and option cards; your choices must be evaluated individually. If required for your application, you may install terminations on your backplane(s). The resulting impedance mismatch must be balanced by the electrical capability of your CPU and option cards to drive the load imposed by the resistors.

Three types of termination may be used: a resistor network, an RC (resistor/capacitor) network; or diode termination. A resistor network provides the required impedance mismatch and results in loading. An RC network does not impose a static load as does a resistor network, but it affects timing. A diode termination is generally used in conjunction with a resistor network to reduce over- and undershoot.

The ISA/PCI backplanes provide termination sockets at the left end of the bus. These sockets accept standard 10-position SIPs manufactured by Bourns and others. Refer to Chapter 2 for more information about bus architecture.

Some signal lines should not be terminated in backplanes having PCI connectors. Table 3-5 lists the control signals that should not be terminated.

Table 3-5: Unterminated Control Signals

ISA Bus Pin Number	Signal	Terminating Resistor
A-1	I/O Channel Check	12-3
B-8	Zero Wait State	12-7
D-1	Memory 16-Bit Chip Select	6-8
D-2	I/O 16-Bit Chip Select	6-9
D-17	Master	4-9

To end signal termination, cut the wire on the terminating resistor for the appropriate signal.

Resistor Termination

Generally, terminations that connect to both +5V and ground work best, although you may have terminations to +5V only. The following two examples illustrate termination in digital signals with Single Inline Pin (SIP) resistors connected to both +5V and ground. The examples specify Bourns part numbers, but you may use equivalent values from other manufacturers.

EXAMPLE 1: 330 Ohms to +5V and 220 Ohms to ground (Figure 3-2)

- Bourns part # 4610X-104-221/331 (low profile)
- Bourns part # 4610M-104-221/331 (medium profile)

EXAMPLE 2: 330 Ohms to +5 and 470 Ohms to ground

- Bourns part # 4610X-104-331/471 (low profile)
- Bourns part # 4610M-104-331/471 (medium profile)

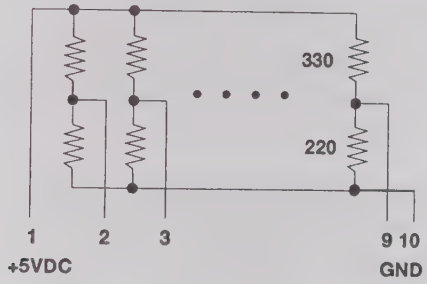

Figure 3-2: Resistor SIP Network

If you read the resistance from the signal pin of the SIP to either pin 1 or pin 10, you will not see the expected resistance of 220 or 330 Ohms. Parallel resistance of other paths prevents the full resistance. For example, the 220 Ohms side will read 143 Ohms (pin 10), and the 330 Ohms side will read 156 Ohms (pin 1). Actual values will vary slightly because of allowed tolerance.

In the examples above, SIPs are inserted with pin 1 toward the back of the chassis. You may reverse the SIP, which is occasionally recommended to improve the shape of the high signal. Other resistor values may be used if problems persist on the bus. Some cards do not operate well on large buses and may require experimentation to isolate intermittent operation.

RC Network Termination

The RC network connects signal lines through a resistor in series with a capacitor to +5V or ground (Figure 3-3). This termination method imposes no static load on the bus; however, increased capacitance on the line will affect timing factors. RC networks are also slightly more expensive than resistors alone.

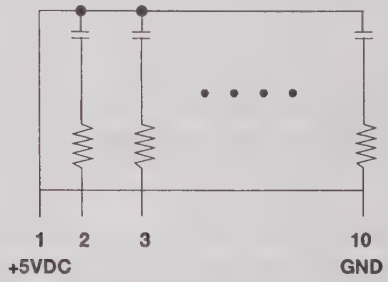

Figure 3-3: RC SIP Network

Diode Termination

Diodes may be connected between the signal lines and both +5V and ground (Figure 3-4). Spikes greater than the +5V rail are shunted and limited to +5V. Negative spikes are shunted to ground. Thus, the bus sees only signals in the range of 0-5V. Diode termination reduces over- and under-shoot, but doesn't improve signal shape or edge times. Diode termination is generally used in conjunction with resistor termination.

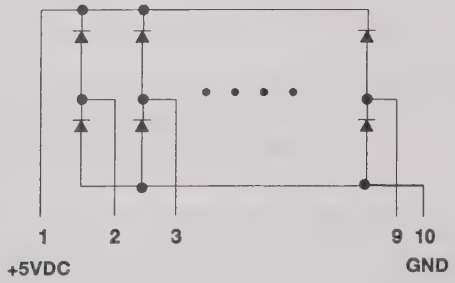

Figure 3-4: Diode SIP Network

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Chapter 4: PCI Bus Overview

This chapter describes the functions and connections of the PCI local bus, a high performance, 32-bit or 64-bit bus with multiplexed address and data lines. The bus serves as an interconnect mechanism between highly integrated peripheral controller components, peripheral add-in boards, and processor/memory systems.

The PCI component with its add-in card interface is processor independent, enabling an efficient transition to future processor architectures. Processor independence allows optimized I/O functions, enables concurrent operation with the processor/memory subsystem, and accommodates graphics plus high-performance peripherals.

Enhanced video and multimedia displays along with other high-bandwidth I/O will continue to increase local bus bandwidth requirements. A transparent 64-bit extension of the 32-bit data and address buses doubles the bus bandwidth and offers forward and backward compatibility of 32-bit and 64-bit PCI local bus peripherals.

The PCI local bus standard provides additional benefits to the users of PCI-based systems. Configuration registers are specified for PCI components and add-in cards. A system with embedded auto-configuration software offers true ease-of-use by automatically configuring PCI add-in cards at power on.

All PCI slots in the ISA/PCI backplanes support bus mastering.

DEC Bridge Chip

The high-performance DEC bridge chip expands the electrical capacity of all PCI systems by allowing more devices than a single PCI bus can support. Each new bridge chip creates an additional PCI bus with a corresponding increase in electrical loads.

The bridge chip has two PCI interfaces. The primary interface connects directly to the PCI bus closest to the host CPU. The secondary interface creates a new, independent PCI bus. Transactions occur between a master on one PCI bus and a target on the other. However, the bridge chip also allows the two PCI buses to operate independently. A master and a target located on the same PCI bus can communicate with each other even if one bus is busy. As a result, the bridge can isolate traffic between devices on one PCI bus from devices on other PCI buses. This feature improves system performance in such applications as multimedia.

PCI Signal Definitions

The PCI interface requires a minimum of 47 pins for a target-only device and 49 pins for a master. These pins handle data and addressing, interface control, arbitration, and system functions. Figure 4-1 shows the pins in functional groups, with required pins on the left side and optional pins on the right. The directional arrows on the signals indicate a combination master/target device.

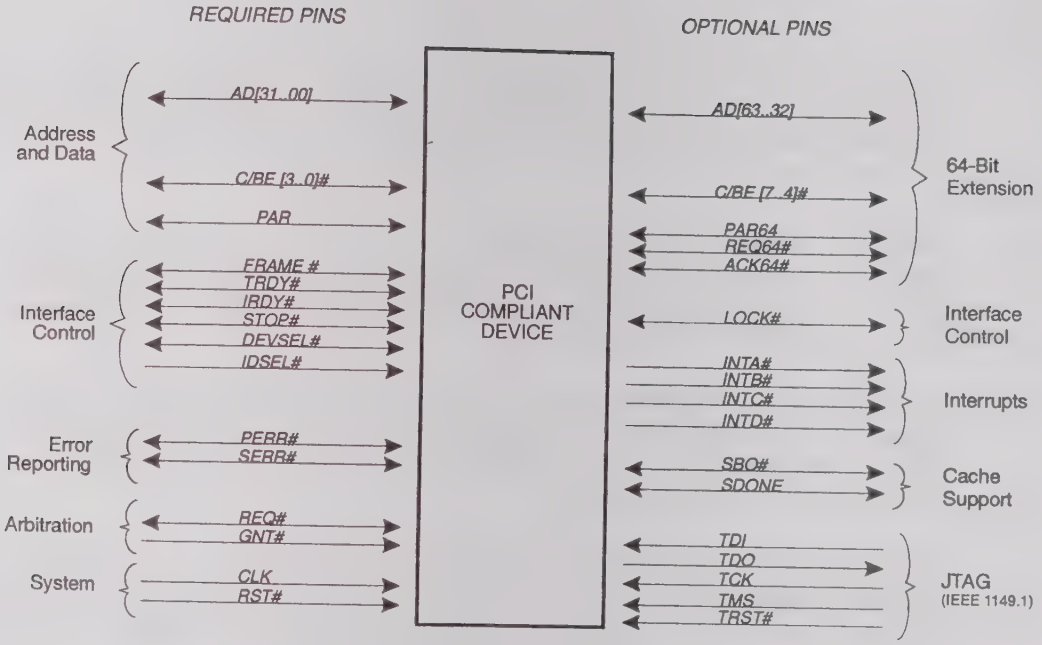

Figure 4-1: PCI Signals

Pin Functional Groups

PCI pin definitions are organized in the functional groups shown in Figure 4-1. A # symbol at the end of a signal name indicates that the signal is active *low*. When the # symbol is absent, the signal is active *high*.

System Pins

CLK — CLocK provides timing for all transactions on the PCI bus and is an input to every PCI device.

RST# — ReSeT brings specific registers, sequencers, and signals to a consistent state.

Address and Data Pins

AD[31..00] — Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts.

C/BE [3..0]# — Bus Commands and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, these pins define the bus command; during the data phase they serve as byte enables. The byte enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/BE0# applies to byte 0 (least significant) and C/BE3# applies to byte 3 (most significant).

PAR — PARity is even across AD[31..00] and C/BE[3..0]#. All PCI agents require parity generation. The master drives PAR for address and write data phases; the target drives PAR for read data phases.

Interface Control Pins

FRAME# — Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAME# indicates the beginning of a bus transaction. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in the final data phase.

IRDY# — Initiator ReaDY indicates the agent's (bus master's) ability to complete the current data phase of a transaction. IRDY# is used in conjunction with TRD#. A data phase is completed on any clock at which IRDY# and TRDY# are sample asserted. Wait cycles are added until both signals are asserted together.

TRDY# — Target ReaDY indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock at which IRDY# and TRDY# are sample asserted. Wait cycles are added until both signals are asserted together.

STOP# — Stop indicates a request from the current target to the master to halt the current transaction.

LOCK# — Lock indicates that an operation may require multiple transactions to complete. When LOCK# is asserted, non-exclusive transactions may proceed to an address that is unlocked. A grant to start a transaction on PCI does not guarantee control of LOCK#. Control of LOCK# is obtained under its own protocol in conjunction with GNT#.

IDSEL — Initialization Device SELect serves as a chip select during configuration read and write transactions.

DEVSEL# — DEVice SELect, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether a device on the bus has been selected.

Arbitration Pins (Bus Masters only)

REQ# — REQuest indicates to the arbiter that an agent needs to use the bus. This is a point-to-point signal. Every master has its own REQ#.

GNT# — GraNT indicates to the agent that access to the bus has been granted. This is a point-to-point signal. Every master has its own GNT#.

Error Reporting Pins

PERR# — Parity ERRor reports data parity errors during all PCI transactions except a Special Cycle. PERR# is sustained tri-state and must be driven active by the agent receiving data when a data parity error is detected.

SERR# — System ERRor reports address parity errors, data parity errors on the Special Cycle command, or any other system error causing catastrophic results. If an agent does not want a non-maskable interrupt to be generated, a different reporting mechanism is required.

Interrupt Pins (Optional)

Interrupts on PCI are optional and defined as level sensitive, asserted low (negative true), and using open-drain output drivers. PCI defines one interrupt for a single function and up to four interrupt lines for a multifunction device or connector.

INTA# — INTA# requests an interrupt. For a single function device, only INTA# may be used, while the other three interrupt lines have no meaning.

INTB#, INTC#, INTD# — These signals request additional interrupts and only have meaning on a multifunction device.

Cache Support Pins (Optional)

Cacheable PCI memory should implement both cache support pins as inputs to allow the PCI to work with either write-through or write-back caches,

SBO# — Snoop BackOff indicates a signal to a modified line when asserted. When SBO# is deasserted and SDONE is asserted it indicates a clean snoop result.

SDONE — Snoop DONE indicates the status of the snoop for the current access. When deasserted, it indicates the result of the snoop is still pending. When asserted, it indicates the snoop is complete.

64-Bit Bus Extension Pins (Optional)

The 64-bit extension pins are collectively optional. That is, if you use the 64-bit extension, all the pins below are required.

AD[63..32] — Address and Data are multiplexed in the same pins and provide 32 additional bits. During an address phase, the upper 32-bits of a 64-bit address are transferred. During a data phase, an additional 32-bits of data are transferred when REQ64# and ACK64# are both asserted.

C/BE[7..4]# — Bus Command and Byte Enables are multiplexed on the same pins. During an address phase, the actual bus command is transferred. During a data phase, they serve as byte enables indicating which byte lanes carry meaningful data when REQ64# and ACK64# are both asserted.

REQ64# — REQuest 64-bit transfer, when actively driven by the current bus master, indicates a need to transfer data using 64 bits.

ACK64# ACKnowledge 64-bit transfer, when actively driven by the target device, indicates the target can transfer data using 64 bits.

PAR64 PARity 64 is the even parity bit that protects AD[63..32] and C/BE[7..4]#. The master drives PAR64 for address and write data phases; the target drives PAR64 for read data phases.

JTAG/Boundary Pins (Optional)

The Joint Test Action Group (JTAG) bus has been defined by IEEE Standard 1149.1. JTAG defines a Test Access Port (TAP) and boundary-scan architecture for integrated circuits. This port has been included as an optional interface for PCI devices. The TAP has four pins (five optional) that interface serially with a TAP controller within the PCI device.

TCK Test ClocK clocks state information and test data into and out of the device during TAP operation.

TDI Test Data Input serially shifts test data and test instructions into the device during TAP operation.

TDO Test Data Output serially shifts test data and test instructions out of the device during TAP operation.

TMS Test Mode Select controls the state of the TAP controller in the device.

TRST# Test ReSeT provides an asynchronous initialization of the TAP controller. This signal is optional in IEEE Standard 1149.1.

PCI Local Bus Pin Assignments

Figure 4-2 shows the bus orientation, noting the first and last pins both sides.

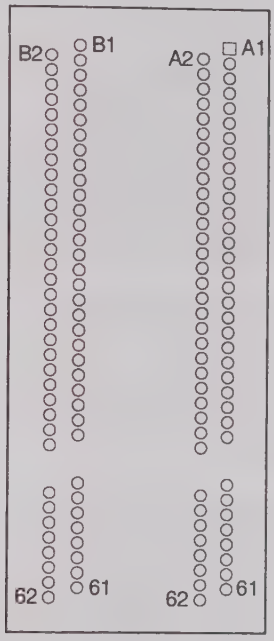

Figure 4-2: Five-Volt 32-Bit Connector

The PCI local bus uses a 5V signaling environment. Table 4-1 shows the bus pin assignments for the 5V connector.

Table 4-1: 32-Bit PCI Local Bus Pin Assignments

I/O Pin	Description
A1	TRST#
A2	+12V
A3	TMS
A4	TDI
A5	+5V
A6	INTA#
A7	INTC#
A8	+5V
A9	RESERVED
A10	+5V
A11	RESERVED
A12	GND
A13	GND
A14	RESERVED
A15	RST#
A16	+5V
A17	GNT#
A18	GND
A19	RESERVED
A20	AD30
A21	+3.3V
A22	AD28
A23	AD26
A24	GNDA24
A25	AD24
A26	IDSEL
A27	+3.3V
A28	AD22
A29	AD20
A30	GND
A31	AD18

I/O Pin	Description
A32	AD16
A33	+3.3V
A34	FRAME#
A35	GND
A36	TRDY#
A37	GND
A38	STOP#
A39	+3.3V
A40	SDONE
A41	SB0#
A42	GND
A43	PAR
A44	AD15
A45	+3.3V
A46	AD13
A47	AD11
A48	GND
A49	AD9
A50	KEY
A51	KEY
A52	C/BE0#
A53	+3.3V
A54	AD6
A55	AD4
A56	GND
A57	AD2
A58	AD0
A59	+5V
A60	REQ64#
A61	+5V
A62	+5V

I/O Pin	Description
B1	-12V
B2	TCK
B3	GND
B4	TDO
B5	+5V
B6	+5V
B7	INTB#
B8	INTD#
B9	PRSNT1#
B10	RESERVED
B11	PRSNT2#
B12	GND
B13	GND
B14	RESERVED
B15	GND
B16	CLK
B17	GND
B18	REQ#
B19	+5V
B20	AD31
B21	AD29
B22	GND
B23	AD27
B24	AD25
B25	+3.3V
B26	C/BE3#
B27	AD23
B28	GND
B29	AD21
B30	AD19
B31	+3.3V

I/O Pin	Description
B32	AD17
B33	C/BE2#
B34	GND
B35	IRDY#
B36	+3.3V
B37	DEVSEL#
B38	GND
B39	LOCK#
B40	PERR#
B41	+3.3V
B42	SERR#
B43	+3.3V
B44	C/BE1#
B45	AD14
B46	GND
B47	AD12
B48	AD10
B49	GND
B50	KEY
B51	KEY
B52	AD8
B53	AD7
B54	+3.3V
B55	AD5
B56	AD3
B57	GND
B58	AD1
B59	+5V
B60	ACK64#
B61	+5V
B62	+5V

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